



GOVERNMENT COLLEGE OF ENGINEERING

Srirangam, Sethurappatti, Tiruchirappalli – 620 012.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

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TWO - DAY NATIONAL LEVEL TECHNICAL WORKSHOP

on

ANALOG IC DESIGN USING CADENCE EDA TOOLS

22-23 AUGUST 2025

14.08.2025

ORGANISING COMMITTEE:

CHIEF PATRON

Dr. V.Gopalakrishnan M.E., Ph.D.

Principal

Government College Engineering Srirangam,
Sethurapatti, Trichy-620 012.

CHAIR

Dr. M. Elangovan, M.E., Ph.D.

Head of the Department

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Government College Engineering Srirangam,
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RESOURCE PERSONS

Mr.V.Navaneethakrishnan

Senior Field Application Engineer,

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Assistant Professor /ECE

PSG College of Technology, Coimbatore.

COORDINATORS

Dr. K. Bommaraju, M.E., Ph.D.

Assistant Professor

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Professor (CAS)

Dept. of Electronics and Communication Engg.
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TECHNICAL SUPPORT

Prof. N. Sri Ramalinga Ganesa Perumal M.E.,

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TECHNICAL STAFF

Mr. P. Kanagaraj & Mr. E. Bharathi

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Government College Engineering Srirangam,
Sethurapatti, Trichy-620 012.

Encl:Brochure.

Dear All,

Sub: Invitation for Two-day National Level Technical workshop – Reg.

We are pleased to inform you that Two-day national level technical workshop organized by the Department of Electronics and Communication Engineering, Government College of Engineering Srirangam, Sethurapatti, Trichy-12 on “Analog IC Design using CADENCE EDA Tools” during 22-23 August 2025.

We request you to kindly participate in the above workshop which is intended to provide the opportunity for students of ECE/VLSI Design who are studying in Engineering Colleges. The Programme will be more fruitful by your presence.

Registration can be done using the link:

<https://forms.gle/hgZDy6MwqzzRYdMM9>

or use QR code.

Selected participants will receive confirmation by email. A registration fee of **Rs. 300/-** to be paid on the spot.



Thanks and Regards,

Coordinators